ABSTRACT OF THE DISCLOSURE

An apparatus and method are provided that enable a computing device to make graceful power state transitions that do no impose unnecessary power surge compensations requirements on associated power sources. The apparatus has power control logic that is configured to determine if the computing device is to enter a low power state. The power control logic includes a plurality of stop signals. Each of the plurality of stop signals sequentially indicates that a corresponding clock signal be stopped, where the corresponding clock signal is operatively coupled to a corresponding sector logic element within the computing device.